Microfabricated electrochemical sensors for combustion applications

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ABSTRACT

A new design for the miniaturization of an existing oxygen sensor is proposed based on the application of silicon microfabrication technologies to a cm sized O_2 sensor demonstrated by Argonne National Laboratory and The Ohio State University which seals a metal/metal oxide within the structure to provide an integrated oxygen reference. The structural and processing changes suggested will result in a novel MEMS-based device meeting the semiconductor industry standards for cost efficiency and mass production. The MEMS design requires thin film depositions to create a YSZ membrane, palladium oxide reference and platinum electrodes. Pt electrodes are studied under operational conditions ensuring film conductivity over prolonged usage. SEM imaging confirms void formation after extended tests, consistent with the literature. Furthermore, hydrophilic bonding of pairs of silicon die samples containing the YSZ membrane and palladium oxide is discussed in order to create hermetic sealed cavities for oxygen reference. The introduction of tensile Si_3N_4 films to the backside of the silicon die generates bowing of the chips, compromising bond quality. This effect is controlled through the application of pressure during the initial bonding stages. In addition, KOH etching of the bonded die samples is discussed, and a YSZ membrane that survives the etching step is characterized by Raman spectroscopy.

Keywords: MEMS-based sensor, oxygen sensor, platinum electrode, adhesion layer, hydrophilic bonding, KOH etch, yttria stabilized zirconia, palladium oxide.

1. INTRODUCTION

There is worldwide concern on the anthropogenic gases released into the atmosphere and the many different ways they might be affecting our planet. As a consequence to these effects we have seen gas emission regulations and standards becoming consistently stricter in the past twenty years. Many industries are seeking ways to more accurately monitor and control combustion processes by getting closer to the heart of the combustion environment, such as that in coal-fired power plants, petrochemical plants, blast furnaces, glass processing equipment, and even inside internal combustion engines. The most common chemical gas sensors for combustion control are potentiometric oxygen sensors. However, real-time oxygen sensing inside combustion chambers have many limitations. There is a high cost for providing external reference air for these sensors as well as the lack of durable high-temperature devices capable of withstanding repeated thermal cycling with temperatures ranging up to 1600°C [1,2,3,4].

Introduction of semiconductor industry-based manufacturing practices to sensor technology has the potential to revolutionize costs as well as make the application of chemical sensors more ubiquitous. However, in the current commercial oxygen sensor design, advantages of miniaturization will not be realized without fundamental changes in design. These include removing the need for an external air reference, thereby eliminating the need for high temperature plumbing and fittings, reducing the overall size of the sensor package, and facilitating the placement of sensors. The recent discovery of an oxygen sensor by Argonne National Laboratory and The Ohio State University with a self-contained reference gas system and a unique deformation bonding method, that does not require intermediate bonding materials and provides unsurpassed oxygen-sensing capabilities, provides a unique opportunity to adapt MEMS-based fabrication technology for designing chemical gas sensors. The novelty in the sensor is the sealing process, which involves a high temperature press that exploits both temperature and pressure to force the zirconia components into their

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neighbors by a phenomenon known as grain boundary sliding [5]. The details of the sensor design are outlined in previously published work [6].
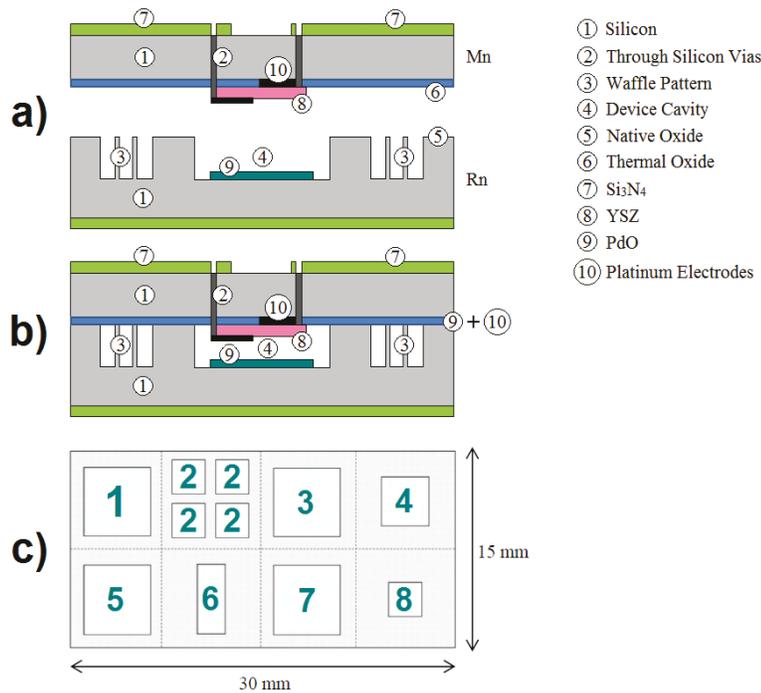
Figure 1 - A schematic of membrane (Mn) and reference (Rn) die with their corresponding microstructures and thin films is shown in a), and the final bonded device is shown in b). The cavity design on the reference die is represented in c).

The existing design of this centimeter-size oxygen sensor has the capacity to withstand temperatures up to 800°C and eliminates the need for costly and bulky high-temperature-resistant external plumbing for a reference air system, making possible the placement of the sensor (or multiple sensors) near the source of combustion for faster and more accurate monitoring of combustion products and a more rapid response for feedback control. However, the technology gap of adapting novel semiconductor industry-based microfabrication techniques for producing chemical gas sensors with the necessary technical and cost attributes required for widespread use within combustion applications needs to be filled. To meet this objective, manufacturing practices for macroscopic ceramic objects have to be translated to the micro and nanometer length scale.

A number of structural and processing differences (relative to the macro device) are required to enable wafer level fabrication. The proposed sensor design is illustrated in Figure 1a. The micro fabricated structure consists of two patterned silicon substrates that are hermetically bonded together through hydrophilic bonding (Figure 1b). A thin film of palladium oxide is sealed in the cavity region of the reference die (Rn) to serve as the oxygen reference. The membrane die (Mn) contains a YSZ membrane with patterned platinum electrodes on both sides. The electrical signal is a Nernst potential generated by differences in pO_2 concentrations in the sealed cavity and external to the sensor. As the Pd metal/PdO metal oxide reduces/oxidizes to maintain the internal pO_2 constant as a function of temperature, oxygen ion conduction creates the Nernst potential across the membrane which is monitored as a function of time.

Through silicon vias (TSV) filled with highly doped polysilicon are used to connect both sets of Pt electrodes to metal traces and bond pads on the (Mn) top-side of the device. The vias are electrically isolated from the surrounding substrate by SiO_2. The TSV approach eliminates the need for Pt traces to pass through bonding regions and simplifies the overall device packaging. Polysilicon-filled TSVs also provide hermetically-sealed electrical connections, with a resistance of less than 10 Ω and are compatible with high temperature processing and operation.

2. EXPERIMENTAL

2.1 Wafer processing

The membrane die originated from 150 mm silicon wafers which were 310 μm thick. The three different membrane die tested had a 50 nm (M1), 25 nm (M2) and 10 nm (M3) layer of thermally grown oxide on the bonding surface. Die types M2 and M3 also had Si_3N_4 film on the backside. The patterned silicon nitride was deposited through LPCVD on the top side to serve as a KOH hard mask. The reference die originated from 150 mm silicon wafer which were 575 μm thick. Three different reference die were tested: a chip with a cavity (R1); a waffle pattern on the wafer also with a cavity (R2);

and a R2 type with a stoichiometric LPCVD Si_3N_4 backside film (R3). The wafer was initially patterned by reactive ion etching (RIE) to create the shallow cavity (R1-R3). Some of the reference wafers also had a waffle pattern created during RIE (R2-R3). All types of reference die had a native oxide on the bonding surface. Photoresist on the backside of the membrane wafer and cover tape over the patterned side of the reference wafer served as protective layers against particles generated during dicing. Each chip after dicing is 30 mm by 15 mm. Each reference die had 8 individual 7.5 mm by 7.5 mm cell designs, depicted 1-8 in Figure 1c.

Sample type	Thickness (μm)	Bonding interface oxide thickness (nm)	Backside Film (nm)	DRIE Pattern
M1	310	50	50 SiO2	N/A
M2	310	25	200 Si3N4 / 50 SiO2	N/A
M3	310	10	200 Si3N4 / 50 SiO2	N/A
R1	575	Native	Native	Cavity
R2	575	Native	Native	Cavity-Waffle
R3	575	Native	300 Si3N4 / 50 SiO2	Cavity-Waffle

Table 1 – Summary of die types tested in this study.

2.2 Thin films

A tantalum adhesion layer was deposited via electron beam evaporation in order to increase the adhesion of platinum to silicon and YSZ. Platinum electrodes were also deposited via electron beam evaporation without breaking vacuum. YSZ was deposited on the top membrane silicon die using a magnetron sputtering system in an argon environment with a power of 200 Watts at 2 mTorr and annealed at 1000°C in argon for 1 hour. The Pd was deposited on the bottom reference die with the same system using a lower power of 40 Watts at 5 mTorr and annealed at 700°C in a mixture of 85% N_2 and 15% O_2 for 4 hours. The YSZ and Pd as-deposited thicknesses were 200 and 30 nm respectively. The targets used for the sputtering of the materials were 99.9% YSZ, 5% weight yttria and 99.95% Pd. For each of the thin films, individually designed shadow masks were used to transfer the desired pattern onto the substrates.

2.3 Hydrophilic bonding

Samples were cleaned with a jet of water prior to resist and cover tape stripping. Dies to be bonded were sonicated in a solution of 1 drop Triton X-100 per 100 mL H_2O. Dies were then rinsed for several seconds with acetone, then held on the opposite side and rinsed with acetone for several seconds again, all with intermittent drying and cleaning the tweezers with acetone in between. This step was then repeated with isopropyl alcohol. Afterwards the samples undergo standard RCA cleaning, which includes one step in a 3:1 H_2SO_4:H_2O_2 solution at 120°C and a second step in a 5:1:1 H_2O:H_2O_2:NH_4OH solution at 70°C. Chips were then activated for 30-40 seconds in a Technics bench top RIE O_2 plasma with an 80-83 mTorr operating pressure at 100-103 Watts. Bonding was initiated after wetting the die with DI water and drying, and brought into contact by pressing the tips of a pair of forceps in the center of the stacked dies to produce the bonded sample. Samples that required pressure during aging were also under pressure up to 310°C, at which point they could be removed and heated to corresponding test temperature 300-1200°C for 2 hours in a conventional oven. Samples that did not require pressure were readily taken to the test temperature for 2 hours after aging. Samples requiring pressure were aged for 12 hours at 52°C and subsequently annealed in an EVG 520HE semi-automated hot embossing system at 310°C.

Scanning acoustic microscope (SAM) images of bonded samples are collected on a Sonix Vision acoustic microscope. The transducer scans at a frequency of 110 Hz at a speed of 150 mm/min resulting in a resolution of approximately 20 μm. A brightness map is created by the WinIC software (by Sonix) using the time of flight of the reflected signal, which corresponds to the density of the material. Higher density areas (bonded interface) are depicted as dark regions while

lower density areas (voids) are displayed as bright regions on the image.. All samples imaged with this technique are oriented as the depiction in Figure 1c.

3. RESULTS & DISCUSSION

3.1 Platinum electrodes

It has been reported frequently in the literature that thin films of Pt degrade at temperatures above 500°C. This degradation leads to an increase in resistance [7,8,9] and hillock or void formation [7,10,11], which eventually leads to electrical failure. Generally, materials such as silicon nitride and silicon dioxide do not form good adhesion with deposited thin films of noble metals such as platinum and gold. However it has been extensively shown that very thin layers of other metals such as titanium, zirconium and tantalum can be used as an adhesion layer between the substrate and the noble metal [7,9,12,13] .
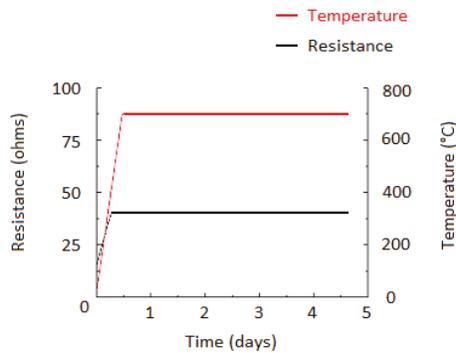
Figure 2 – The graph shows the resistance over time of an individual Pt/Ta electrode on Si at 600°C in air.

For high temperature applications, another factor has to be considered. Due to their less noble nature, adhesion layer metals tend to be the cause of failure of thin platinum electrodes. Titanium has been studied as an adhesion layer and showed good adhesion for temperatures ranging from room temperature to 550°C in air [14,15,16]. But films treated at higher temperatures showed decreasing adhesive quality, and above 800°C there was extensive loss of adhesion [14]. Tantalum on the other hand is a much more adequate material for high-temperature adhesion layers. In the same work, Tiggelaar et al. shows that Pt/Ta films were able to withstand temperatures up to 950°C with excellent adhesion, comparable to the as-deposited films.

Given the beneficial adhesive properties of tantalum to Si substrates and Pt thin films, Ta was chosen as the adhesion layer for the platinum electrodes in this study. Although the Pt/Ta electrode system seemed to be the most suitable for our application, these films still have a non-infinite lifetime and degrade over extensive high temperature exposures. Pt/Ta films tend to preserve their smooth surfaces for temperatures up to 550°C in any type of environment [14]. As temperatures go above this threshold hillocks begin to form, and after extensive high temperature exposures they flatten and voids begin to appear. These voids then grow over time and start to perforate the film, eventually causing the formation of individual metal islands and breakdown of the electrical conductivity of the system. Higher temperatures tend to promote faster hillock and void formation, but the amount of time the films are exposed to these harsh environments seem to be the major factor [14]. Firebaugh et al. also demonstrated that the thickness of the adhesion layer as well as the thickness of the platinum greatly influence the lifetime of the film. Samples with Ta adhesion layer of 10 nm had the longest lifetimes, while for platinum thicker films survived the longest. For these reasons, a Ta adhesion layer of 10 nm and a Pt thickness of 200 nm was chosen for the electrodes in this study.

Throughout the fabrication steps and final application of the proposed device the electrodes are exposed to different gas environments and different temperatures. Tests were conducted in order to confirm the extended lifetime of the platinum electrodes and eliminate the possibility of void formation in the films from being the failure mechanism of the sensor. Figure 2 shows the results of a four day exposure of the Pt/Ta film on silicon to air at 600°C. After the initial ramp
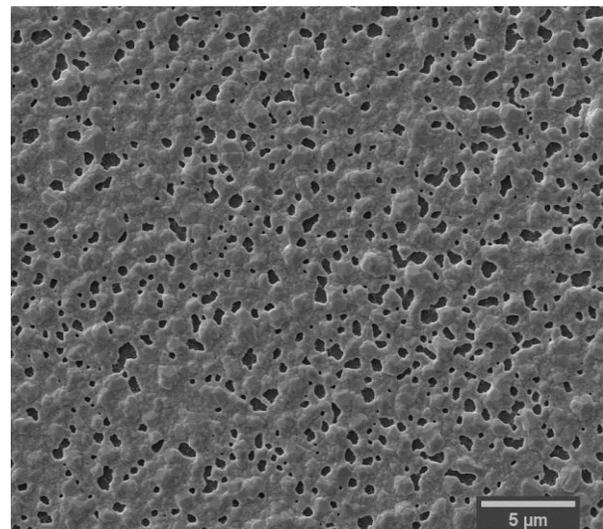
Figure 3 – SEM image of a Pt/Ta electrode after the extended resistance study depicted in Figure 2. Initial void formation is present, which is the primary cause of Pt/Ta thin film degradation and consistent with the literature.

up stage, the resistance through the film became nearly constant with a slight increase over time. SEM imaging confirmed the initiation of void formation as expected (Figure 3). The experiment was repeated with a new sample at 700°C in a nitrogen environment and the increase in resistance over the period of six days was less than 5 ohms (data not shown). Electrodes were also deposited onto YSZ films and tested at 600°C in air and 700°C in nitrogen. For both environments, no resistance change was detected after four days of exposure.

3.2 Hydrophilic bonding

In order to create the enclosed cavity with the reference partial pressure of oxygen, a hermetic bond between top and bottom die must be accomplished. The hermeticity of the bond is crucial since the internal partial pressure of oxygen generates one of the electrical potentials on the YSZ membrane to be measured. Any leakage would result in erroneous sensing measurements. Although grain boundary sliding was used to seal the original macro-scale Ohio State device, initial studies on this bonding technique for thin YSZ films on silicon showed that large macroscopic damage was being caused to the sides opposite to the bonding interface.

As an alternative, hydrophilic bonding to produce silicon wafer-based devices is a well-documented and very attractive technique because it can be initiated at room temperature and annealed to as low as 200 – 300°C [17,18] making the bonding method more versatile than the hot pressing methods mentioned before. The initial bonding takes place after the surfaces have been extensively cleaned and activated. The treated silicon dioxide surfaces are left with OH groups chemically adsorbed to the silicon [19]. After a DI water rinse and dry step, monolayers of water are physically adsorbed onto the surfaces, and as the initial contact is made the surfaces bond according to (1) [19]. At temperatures up to 400°C the water molecules dissociate forming oxide (2) [20]. Once the samples are annealed above 400°C OH groups begin to disappear forming silicon to oxygen bonds (3) [19,20]. The water molecules resulting from reaction (3) further assist bonding by diffusing through the oxide layer and reacting with the bulk silicon [19].

$$Si - OH \ldots nH_2O \ldots HO - Si \qquad (1)$$

$$-Si - Si - + H_2O \rightarrow -Si - O - Si + H_2 \qquad (2)$$

$$Si - OH + HO - Si \leftrightarrow Si - O - Si + H_2O \qquad (3)$$
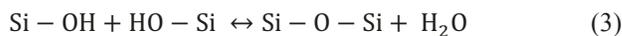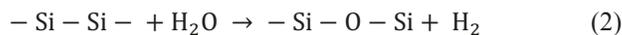
The hydrogen gas produced during (3) diffuses back to the interface forming pockets of H_2 gas and is the main cause of annealing voids, preventing hermetic bonding and greatly affecting bond quality [19,21]. Figure 4 shows SAM images of a hydrophilic bonded sample using M1 and R1 chip types. This sample was aged at 50°C for 2 days then subsequently annealed for two hours and imaged at 300°C (4a), 600°C (4b), 900°C (4c) and 1200°C (4d). The squared white shapes in the images are the RIE drilled cavities described earlier. The circular white shapes are H_2 gas voids at the bonded interface formed after annealing. These voids seem to merge as the samples are annealed up to 900°C, which is consistent with previous results [19,21]. Temperatures above 900°C allow the hydrogen to diffuse away from the interface causing the voids to diminish and even disappear [22], and can be confirmed on Figure 4d. Although the 1200°C anneal enhanced bonding, there is still a significant amount of voids. Also, temperatures above 900°C are not compatible with the electrode design and hence must be avoided. The presence of these gas voids can compromise the integrity of the hermetic seal and have the potential to breach the device.

One of the methods for preventing gas voids from forming is to keep anneal temperatures under the percolation threshold (below 300°C) [17,18]. In our case this is not possible since the temperature range of operation is well above this limit. As an alternative, additional cavities in the bonded interface can provide space for hydrogen to diffuse into rather than agglomerating at the interface [23,24,25]. Additional to the cavities in reference chips R1, a waffle pattern was designed and implemented into reference chips R2 and R3 in order to create space for hydrogen diffusion. The use of similar

Figure 4 - Sample bonded from M1 and R1 and SAM imaged after annealing at 300°C (a), 600°C (b), 900°C (c) and 1200°C (d).

Figure 5 - Sample bonded from M1 and R2 and SAM imaged after annealing at 300°C (a), 600°C (b), 900°C (c) and 1200°C (d).

microstructures for the same application has been previously reported [23]. The maximum partial pressure of H_2 within cavities with similar design to the mentioned waffle pattern was measured to be 0.16 atm. Figure 5 shows SAM images of bonded M1 and R2 chips after annealing at different temperatures. The crosshatch areas around the cavities are the waffle pattern, and the dark lines indicate where the flat silicon surfaces bonded. After annealing at 300°C (5a) good bond was achieved throughout most of the sample, although poor bonding can be noticed around the edges. The absence of voids indicates that the hydrogen generated during annealing was able to diffuse into the waffle pattern. At 600°C (5b) there is a significant improvement in bonding particularly at the edges, although inferior bond quality can still be seen where the sample was held by the forceps during bonding. After annealing at 900°C (5c) bonding seemed nearly uniform. The 1200°C step (5d) was realized for consistency.

The use of Si_3N_4 layers on the backside of the membrane and reference chips was also studied. The nitride layer serves as a KOH hard mask in order to create the opening on the membrane chip to expose the YSZ membrane and as a protective layer for the backside of the reference chip. The introduction of a tensile Si_3N_4 film induces a bowing of the substrate as the system relaxes. When attempting to bond M2 with R3 chips, the edges of the sample would clearly not establish good bond quality even after high temperature anneals. Regions closer to the center seemed to establish better bonding. In the past, 0.5 mm thick, 4'' diameter silicon wafers have been successfully bonded with a bow of approximately 25 μm [26]. For comparison, the effective bowing of the 30 mm cross-section in M2 and R3 chips was 87 μm and 51 μm respectively after fitting the parabola and extrapolating to a 4'' diameter.

In order to overcome this issue a slightly modified bonding method was developed. For this procedure, pressure was applied during aging and the first stages of annealing. Initial bonding is established at room temperature, and afterwards the sample was placed under 5 MPa of compressive stress before being annealed at 310°C for 2 hours. Afterwards the sample is annealed up to 1200°C without pressure. This procedure was sufficient to establish a good bond throughout the bonding interface without development of macroscopic defects, as it had been accomplished before without the nitride layer. This method has also been used to bond membrane chips (M2) with a YSZ layer and reference chips (R3) with a PdO layer, which will be required for the eventual full development of the sensors (Figure 1b). More details on the bonding method used in this work have been reported in a separate publication [27].

3.3 KOH etch and YSZ membrane fabrication

Subsequent to bonding, each device undergoes a KOH etching step in order to remove material from the top die and expose the YSZ membrane. Potassium hydroxide etching is a standard wet-etching procedure widely used to etching single crystal silicon wafers. The KOH solution reacts with silicon atoms in the [100] and [110] directions removing material at rates on the order of μm/min while etching extremely slowly in the [111] direction [28,29]. Studies on the KOH etching of bonded samples showed significant damage caused to the bonded structures. Samples with poorly bonded edges suffered extensive side etching, compromising the integrity of the hermetic seal. Figure 6 shows SAM images of a M2 and R3 bonded chip before and after etching. In Figure 6b it becomes evident that both cavities on the left hand side were damaged during etching (region 1). The dark regions over the cavities represent the areas on the membrane chip that were etched away. On the right hand side there is also etching damage, compromising the bottom cavity (region 2). Both of these areas had poor bond quality prior to etching (Figure 6a). Other areas in the sample

Figure 6 – SAM images of M2 and R3 bonded chips before (a) and after (b) KOH etching.

Figure 7 – a) Optical image of a YSZ membrane that partially survived KOH etching. Label 1 corresponds to an area on the membrane where exposed YSZ is localized, which has been confirmed with Raman spectroscopy (b). Label 2 shows an area where the silicon did not fully etch.

where bonding was more uniform were not damaged.

Initial tests of KOH etching of bonded samples containing YSZ and PdO have also been accomplished. Due to similar damage seen in Figure 6b the surviving cavity yield has been low, approximately 20-30%. Figure 7a shows an optical image of a YSZ membrane that partially survived the etching step. Except from the top right corner, the integrity of the membrane looks promising. Raman spectroscopy of Area 1 in this image confirmed the presence of exposed YSZ (Figure 7b), although a silicon signal was detected indicating residual Si. Other regions of the membrane still contain silicon covering the YSZ (Area 2).

Other factors can also worsen KOH side etching, for instance the damage caused to the die edges while dicing. In order to increase yield and protect the bonded samples from side etching a variety of additional processing steps are being considered. There is a polymeric protective coating available in the market, of which the effectiveness has been reported [30], with the purpose of protecting integrated circuits structures from KOH etching. Polymethyl methacrylate (PMMA) has also been used as a hard mask for potassium hydroxide etching [31]. The application of one of these coatings could be adapted to the sidewalls of the bonded samples serving as an etch barrier. Another alternative is the use of a PECVD oxide/nitride layer in the attempt to cover the sidewall gaps present due to poor bonding. Although this issue is present at the die level, it is important to note that there are industry standards for wafer level sidewall protection during wet etching and hence this problem would not be present in future wafer-level production.

4. CONCLUSION

A novel design for wafer-level fabrication of an oxygen sensor has been proposed that leverages semiconductor industry microfabrication equipment and processes. The design is based off an existing oxygen sensor developed by Argonne National Laboratory and The Ohio State University. The production of platinum electrodes using tantalum as an adhesion layer was presented, and the quality of conduction throughout extended testing at operational conditions was assessed. Through SEM imaging it was found that the electrodes degrade over prolonged usage, which is consistent with the literature. Although this degradation would eventually cause the electrodes to fail, it was shown that at the harshest operational conditions they were able to continue to operate with minimum resistance changes over the course of several days. Additionally, hydrophilic bonding was established at the die level in order to create hermetic sealed cavities. The formation of H_2 gas voids during subsequent annealing was discussed, and a microstructural change to the reference die at the bonding interface was shown to avoid the formation of voids to occur. The bonding of die samples containing a backside layer of tensile Si_3N_4 was also discussed, and a slightly modified bonding method was presented in order to overcome bowing of the chips by the nitride. Preliminary studies on the KOH etching of bonded samples showed etching damage occurs through the bonding interface. Although some cavities had their hermetic seal broken during etching, a number of cavities were able to survive and a YSZ membrane that partially survived the etching step was characterized via Raman spectroscopy. The usage of additional processing steps will be assessed in order to prevent side etching from occurring.

5. ACKNOWLEDGMENT

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